REMARKS

This paper is filed in reply to the action mailed March 25, 2004. The applicant asks that all claims be allowed in view of the foregoing amendments and the following remarks.

1. Response to Objections Under 37 CFR 1.75(c)

Claims 11-14 are objected to as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. Claims 11-14 have been amended to depend only from claim 2. The applicant believes that the amendments to these claims overcome the Examiner's objection.

Claims 5-6 are objected to as being in improper form because a multiple dependent claim cannot depend from another multiple dependent claim. Claim 5 has been amended to depend only from claim 1. The applicant believes that the amendments to these claims overcome the Examiner's objection.

2. Response to Rejections Under 35 U.S.C. 102(e)

Claims 1-6, 9, and 11-41 stand rejected under 35 U.S.C. 102(e) as being anticipated by Satou et al., U.S. Patent 6,101,584. Applicant respectfully traverses the rejection.

a. Claims 1-6, 9, and 11-14

Amended claim 1 recites a method for controlling access to a dynamic random access memory (DRAM), arranged in a computer system having a processor and memory controller. The method comprises performing, for each DRAM access, a predetermined number of DRAM control operations in response to a corresponding sequence of control instructions included in microcode instructions of the processor.

Satou relates to a computer system that includes a memory and a CPU for making interlock access to the memory. The computer system comprises a CPU 110, a DRAM 120, a cache 130, a clock unit 140, and external bus interface 150 and a memory controller 160 as well

as various bus and control interfaces. Satou discloses a memory controller that prevents the DRAM from being externally accessed while the CPU performs an interlock access.

The CPU generates a number of signals such as REQF, REQO, AF, AO, LOCK, OPR/W to the memory controller and receives corresponding acknowledgement and end signals from the memory controller. However, since the memory system of Satou includes both a DRAM and a cache memory, *the CPU does not know in advance which type of memory access to be performed* by the memory controller. This means that in the computer system of Satou, the memory accesses can never be controlled directly by the CPU, but rather is controlled by the memory controller.

In most modern computer systems, the main memories are often relatively slow with rather long access times and are considered as the bottlenecks of the computer systems. In this context, it is important to keep in mind that faster memory components are generally much more expensive than the slower memory components used as main memories. A common way of alleviating this problem is to use one or more levels of small and fast cache as a buffer between the processor and the larger and slower main memory, as done in Satou.

A cache memory contains copies of blocks of data/instructions that are stored in the main memory (from col. 7, line 66 to col. 8, line 2). In the cache, these blocks of data/instructions correspond to cache line data fields. As reads to the main memory are issued in the computer system, the system first goes to the fast cache to determine if the information is present in the cache. If the information is available in the cache, a so-called cache hit, access to the main memory is not required and the required information is taken directly from the cache. If the information is not available in the cache, a so-called cache miss, the data is fetched from the main memory into the cache, possibly overwriting other active data in the cache. Similarly, as writes to the main memory are issued, data is written to the cache and copied back to the main memory.

In the system of Satou, the memory controller receives a simple request REQF for instruction fetch access or a request REQO for operand data access from the CPU, together with corresponding memory address signals AF and AO, respectively (col. 7, lines 55-66). In response to e.g. a request REQF for fetching instruction codes into the CPU from the memory

system, the memory controller 160 generates a control signal CTRLD for causing the DRAM to perform a read or write operation, or a control signal CTRLC for causing the cache memory to perform a read or write operation. However, as mentioned above, the CPU itself does not know if the access will take place in the cache or in the DRAM. The memory access control is initiated by the CPU as a *general request signal*, but the actual control of the memory accesses is performed exclusively by the memory controller, for example as described on col. 13, lines 7-21 of the Satou patent. With reference to an instruction fetch request, instructions are then finally fetched from the cache or DRAM or external memory and stored in the instruction queue 110a.

Therefore, Satou does not disclose the invention recited in claim 1. The control signals CTRLD or CTRLC used in Satou are not included in any instruction of the processor, but are generated by the memory controller. The computer system of Satou does not perform a sequence of DRAM control operations in response to a corresponding sequence of control instructions included in microcode instructions of the processor.

In addition, the instructions stored in the instruction queue 110a of Satou are not microcode instructions, but rather higher-level machine instructions fetched from external memory or the DRAM for subsequent *decoding* and execution by the CPU. As to the technical meaning of "microcode instructions", microcode is the lowest-level instructions that directly control a microprocessor. A single machine code instruction typically translates into several microcode instructions. In some microprocessor architectures, the microcode is hardwired and cannot be modified, whereas other microprocessor architectures utilize programmable microcode. In the latter case, the microcode may be stored in EEPROM, which can be modified.

It should thus be clear that there is no indication whatsoever of any microcode program holding microcode instructions in Satou, and hence Satou does not disclose any sequence of control instructions included in the processor's microcode instructions for the purpose of controlling access to a primary memory such as a DRAM. Therefore, Satou does not disclose a correlation between the sequence of control instructions of the processor and the DRAM control operations. In Satou, the CPU does not even know if there will be a DRAM access, since the memory controller may find the information directly in the cache. Hence, the CPU of Satou

generates this signal without knowing if it will affect the DRAM, and so there can be no correlation between this signal and a sequence of DRAM control operations.

The flexibility offered by the microcode controlled memory access of the invention, enables the microcode program to freely use so-called page mode. This means that with the invention there is generally no need for a cache memory since the activated row of the DRAM will act as "cache memory".

Even if the general request signal, such as REQF for instruction fetch, of Satou should be interpreted as a control instruction, this request signal is not included in any microcode instruction or in any instruction whatsoever. It is merely a request signal generated by the CPU whenever instructions need to be fetched from memory or the execution requires an operand from memory.

Because Satou fails to disclose at least these limitations of claim 1, the reference cannot anticipate that claim. For at least these reasons, claim 1 is allowable over Satou. Claims 2-6, 9, and 11-14 depend either directly or indirectly from claim 1 and are therefore allowable for at least the same reasons.

b. Claims 15-23

Amended claim 1 recites a controller for a dynamic random access memory (DRAM), in a computer system having a processor. The DRAM controller is responsive to a sequence of control instructions for controlling access to the DRAM, where each control instruction is included in a microcode instruction of a processor.

Claim 15 is allowable over Satou for at least the same reasons as claim 1. Claims 16-23 depend either directly or indirectly from claim 15 and are therefore allowable for at least the same reasons.

c. Claims 24-28

Amended claim 24 recites a computer system having a processor, a primary memory cooperating with the processor, and a memory controller for the primary memory. The memory controller is responsive to a sequence of control instructions from the processor for controlling

access to the primary memory, where each control instruction is included in a microcode instruction of the processor.

Claim 15 is allowable over Satou for at least the same reasons as claim 1. Claims 16-23 depend either directly or indirectly from claim 15 and are therefore allowable for at least the same reasons.

d. Claims 29-35

Amended claim 29 recites a method for performing a virtual direct memory access (DMA) to a memory in a computer system. The method comprises storing data from/to an input/output device in a buffer, transferring the data between the buffer and the primary memory via internal paths of a processor of the computer system, where the data transfer is controlled by a microcode instruction program of the processor.

Claim 29 is allowable over Satou for at least the same reasons as claim 1. In addition, claim 29 is allowable over Satou for at least the following additional reasons. The Examiner interprets the buffer of claims 29 and 36 as the internal register 110d of the CPU in Satou. The DMA buffer of the invention is used by peripheral input/output devices to store data, whereas the register 110d of Satou is occupied with data required for the CPU's execution of instructions. Satou does not disclose a filter for storing data from/to an input/output device because the content of the register 110d in Satou must be kept intact during a DMA transfer and can consequently not be used for storing data to/from any input/output devices. The Examiner also interprets the microcode program proposed by the invention for controlling the data transfer between the DMA buffer and the primary memory as the instruction queue 110a. The instruction queue 110a is a prefetch buffer that stores higher-level machine instructions in turn for execution by the CPU. As previously discussed, there is no mention or any suggestion whatsoever of any microcode instruction program in the Satou patent.

Claims 30-35 depend either directly or indirectly from claim 15 and are therefore allowable for at least the same reasons.

e. Claims 36-41

Amended claim 36 recites a computer system having a processor and a primary memory coupled to the processor. The computer system comprises a buffer for storing data from/to an input/output device, and means for transferring data between the buffer and the primary memory via internal paths of the processor under the control of a microcode instruction program in the processor.

Claim 36 is allowable over Satou for at least the same reasons as claim 29. Claims 37-41 depend either directly or indirectly from claim 36 and are therefore allowable for at least the same reasons.

Please apply the extension fee of one month in the amount of $55.00 and any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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